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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,766	01/18/2002	William P. Cornelius	04860.P2676	5545

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EXAMINER	
PATEL, ANAND B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,766	CORNELIUS, WILLIAM P.	
	Examiner	Art Unit	
	Anand Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22 and 24* is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 3/17/05 has been entered. Claim 23 has been canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5, 7-10, 12, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostrom as applied above and to US Patent No 6327663 to Isaac et al (Isaac).

- As per claim 1, Ostrom discloses an apparatus in a data processing system (paragraph 7, lines 1-2), said apparatus comprising:
  - A voltage controller (110) having an output ("V_{out}") and being coupled to received a signal indicating a level of voltage (paragraph 30, lines 1-6, lines 22-24), and
  - A detector of power change coupled to said voltage controller (120) to provide said signal in response to a change in power level in said data processing system (paragraph 30, lines 1-6).

  Ostrom fails to disclose an apparatus that compensates for voltage drops at the processor by applying more voltage. Isaac discloses an apparatus that adjusts the voltage applied to the processor during powering up, thereby compensating for any loss in voltage (column 2, lines 55-61). This allows the apparatus to stabilize its voltage when a voltage drop has been detected. It would be obvious to one of ordinary skill in the art at the time of

invention to combine the teachings of Ostrom and Isaac to compensate for a voltage drop. The motivation to combine in column 2, lines 61-67, allows the system to compensate for changes automatically so as to avoid stress and damage to the processor.

- As per claim 2, Ostrom discloses an apparatus wherein said voltage controller is coupled to receive a signal to boost voltage (paragraphs 29, lines 7-12; paragraph 31, lines 1-3) and wherein said apparatus compensates for a potential voltage droop.

Ostrom fails to disclose an apparatus that compensates for voltage drops at the processor by applying more voltage. Isaac discloses an apparatus that adjusts the voltage applied to the processor during powering up, and thereby compensating for any loss in voltage (column 2, lines 55-61).

- As per claim 3, Ostrom discloses an apparatus wherein said voltage controller is coupled with a power distribution bus (figure 1, unlabeled connection between 110 and 140) and wherein said detector of power change detects a change in one of current or voltage (paragraph 30, lines 1-6).
- As per claim 5, Ostrom discloses an apparatus wherein said detector of power change is coupled to a microprocessor (paragraph 7, lines 1-2) and said voltage controller and said detector of power change detects a change in current drawn from said microprocessor (paragraph 34, lines 1-6).
- As per claim 7, Ostrom discloses an apparatus wherein said detector of power change may comprise a hardware or a software current detector (200).
- As per claim 8, Ostrom discloses a method for providing a supply of power in a data processing system (paragraph 7, lines 1-2), said method comprising:

- Detecting a change in current drawn by said data processing system (paragraph 34, lines 1-6)
- Determining according to the change in current a power level (paragraph 31, lines 1-14; it should be noted that the determination of a preset output voltage inherently suggests the determination of a preset power level)
- Increasing a voltage level for a predetermined amount of time (paragraphs 31; paragraph 32, lines 1-8).

Ostrom fails to disclose an apparatus that compensates for voltage drops at the processor by applying more voltage. Isaac discloses an apparatus that adjusts the voltage applied to the processor during powering up, and thereby compensating for any loss in voltage (column 2, lines 55-61).

- As per claim 9, Ostrom discloses a method wherein said change in current is detected at a microprocessor (paragraph 34, lines 1-6) to determine whether an increase in demand for power is occurring (paragraph 29, lines 7-12).
- As per claim 10, Isaac discloses a method wherein said method is used to compensate for a voltage droop in said data processing system (column 2, lines 55-61).
- As per claim 12, Ostrom discloses a method wherein a voltage controller is coupled to receive a current level signal (paragraph 34, lines 1-6) and said voltage controller adjusts said voltage level based on said current level signal (paragraphs 31, lines 7-9; paragraph 34, lines 1-9).
- As per claim 14, Ostrom discloses a method wherein said voltage controller, in order to neutralize any voltage droop that can occur, increases the voltage level at the microprocessor

for a limited time up to a predetermined voltage level (paragraph 31, lines 6-14; paragraph 32, lines 1-6).

- As per claim 15, Ostrom discloses a method wherein said voltage controller after a limited time has elapsed decreases the voltage back to within normal parameters (paragraph 32, lines 1-6)

4. Claims 4, 6, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostrom and Isaac as applied above, and in view of US Patent No 5774736 to Wright et al (Wright).

- As per claim 4, Ostrom discloses an apparatus wherein said voltage controller comprises an reference voltage (633) coupled to receive a signal from said detector of power change (634). Ostrom fails to disclose a reference voltage that is adjustable. Wright discloses an adjustable reference voltage (column 10, line 65 – column 11, line 2) that is used to supply power to a CPU. The adjustable reference voltage allows the apparatus to boost power according to the drop in voltage at the processor. It would have been obvious to one of ordinary skill in the art at the time of the invention to allow for an adjustable reference voltage in order to supply different voltage levels to the CPU (column 1, lines 66-67). The combination would thus allow for an adjustable reference voltage to supply extra power to the processor in order to compensate for a voltage droop.
- As per claim 6, Ostrom discloses an apparatus wherein a reference voltage is coupled to provide a voltage level reference according to said signal from said detector of power change (figure 6, claim 52). Ostrom fails to disclose a reference voltage that is adjustable. Wright discloses an adjustable reference voltage (column 10, line 65 – column 11, line 2) that is used to supply power to a CPU.

- As per claim 13, Ostrom discloses a method wherein a reference voltage is coupled to the voltage controller (figure 6) to receive said current level signal and determine said voltage level, which the voltage controller is to provide via a power distribution bus to said microprocessor (figure 5). Ostrom fails to disclose a reference voltage that is adjustable. Wright discloses an adjustable reference voltage (column 10, line 65 – column 11, line 2) that is used to supply power to a CPU.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ostrom and Isaac as applied above, and in view of US Patent No 6580597 to Kanouda et al (Kanouda).

- As per claim 11, Ostrom discloses the method of claim 10 as stated above. Ostrom fails to disclose using the compute load as an indicator of current level change. Kanouda discloses a method wherein determining a change in compute load acts as an indicator of the change in current level (column 5, lines 56-59; column 7, lines 24-28). The ability to use computational loads as an indicator of processor power drain, allows the computer to schedule tasks in a way as to anticipate and prepare for more intensive applications that require more power. Thus the processor voltage can be kept at a steady level rather than having the power supply system compensate for power spikes (column 7, lines 24-28). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the ability to use compute load as an indicator of processor power drain in order to better prepare and adapt to power demand from the processor and avoid spikes and droops.

6. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostrom and Isaac as applied above, and further in view of Kanouda as applied above, and US Patent No 5623647 to Maitra.

- As per claim 16, Ostrom in view of Isaac and Kanouda fails to disclose using programmable units within the system to anticipate changes in compute load at the processor. Maitra discloses a method for programming a microprocessor in said data processing system with instructions to anticipate changes in compute load levels (column 2, lines 43-49). Maitra uses control and scheduling units in order to anticipate when more intensive applications will be run. According to this scheme, the processor will accordingly adjust to either higher or lower frequency states. Again, being able to anticipate changes in power requirements of the processor allows for more efficient task scheduling and more gains in power consumption. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine these two systems in order to anticipate the running of an intensive application, and to thus be able to compensate for the power drain at the processor.
- As per claim 17, Maitra discloses the use of programmed control units to anticipate changes in compute load (column 2, lines 43-49), which are coupled with current level changes (column 7, lines 19-53). The use of a specific frequency per program obviously suggests that a specific power is to be supplied to the processor specific to each program, thus causing the power efficiency called for in the reference.
- As per claim 18, Maitra discloses the use of programming instructions (110, 120, 130) to relay a change in processor power demand. Ostrom discloses the use of a sense circuit to send information about changes in load current levels to a voltage regulator (paragraph 34, lines 1-6).

- As per claim 19, Ostrom discloses the method wherein a voltage controller is coupled to receive a signal (paragraph 30, lines 1-6, lines 22-24) and the voltage controller determines the voltage level needed to be supplied via a power distribution bus to the microprocessor (paragraphs 31, lines 7-9; paragraph 34, lines 1-9).
- As per claim 20, Ostrom discloses the method wherein a voltage controller, in order to neutralize any voltage droop that may occur, increases the voltage level for a limited time up to predetermined voltage level (paragraphs 31; paragraph 32, lines 1-8).
- As per claim 21, Ostrom discloses the method wherein a voltage controller after a limited time has elapsed decreases the voltage back to within normal parameters (paragraph 32, lines 1-8).

Allowable Subject Matter

7. Claims 22-24 allowed. Applicant has combined the allowable subject matter of canceled claim 23 into the body of independent claim 22 as advised in the previous Office Action.

Response to Arguments

8. Applicant's arguments filed 3/17/05 have been fully considered but they are not persuasive.

9. Applicant argues that Ostrom does not indicate that the voltage controller prevents power droop. Examiner disagrees. Although Ostrom does not explicitly recite preventing power droop as an intended function, the prior art is used to compensate for a loss in voltage of a system during a change in states, and thus necessarily prevents power droop when more power is required by the system.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Patel whose telephone number is (571) 272-7211. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ABP

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